Amendments to the Specification

1. Please amend page 9, lines 19-28 of the specification as follows:

FIGs. 3 and **4** are a cross-sectional view of a portion of devices according to certain embodiments of the present invention. As seen in **FIG. 3**, the spacer region **40** is provided by removing portions of the epitaxial layers **12** and **14** to provide mesas **60** corresponding to the active areas of the device. The gate conductor [[**20**]] **24** is provided on the mesa of the epitaxial layers **12** and **14** and continues down sidewalls of the mesa onto the substrate and to the next mesa. The source **20** and drain **22** conductors are air bridged between the mesas **60**. Parasitic capacitances may be reduced and/or minimized by employing air bridges or dielectric crossovers to span the thermal spacer regions **40** with the source and drain electrodes **20** and **22**. The gate electrode **24** could also be air bridged, but space constraints in the layout may prohibit this.

2. Please amend page 10, line 23 - page 11, line 3 of the specification as follows:

Furthermore, in addition to the incorporation of thermal spacers, the pitch between the gate fingers **24** may be non-uniform. For example, the pitch may vary from a small pitch to a larger pitch toward the center of the device. By increasing the pitch at the center of the device, the increased heat dissipation area may compensate for the decreased thermal gradient at the center of the device such that the junction temperature associated with the respective gate fingers may be moderated. A more uniform junction temperature may provided for a decreased peak junction temperature which may result in improved reliability over a conventional uniform spaced device under the same operating conditions. Furthermore, the more uniform thermal profile may reduce impedance differences between the fingers and, thereby, improve linearity of an RF device. Thus, embodiments of the present invention may include a non-uniform gate pitch as described in United States Patent Application Serial No. [[_____]] 10/734,398, entitled "NON-UNIFORM GATE PITCH

SEMICONDUCTOR DEVICES," ~~(Attorney Docket No. 5308-376),~~ the disclosure of which is incorporated herein by reference as if set forth in its entirety.

3. Please amend page 5, lines 15-17 of the specification as follows:

FIG. 5B is a thermal model of a divided gate finger device corresponding to the unitary gate finger device of **FIG. 5A** according to embodiments of the present invention; and

FIG. 6 is a plan view of a portion of a multi-cell transistor according to further embodiments of the present invention.

4. Please amend page 10, lines 13-22 of the specification as follows:

Furthermore, while the thermal spacers of **FIGs. 1** through **4** are illustrated as having the same number of spacers in each gate finger, differing numbers of spacers may be provided in different fingers. For example, as illustrated in FIG. 6, a checkerboard pattern 80 of spacers may be provided where adjacent fingers having differing numbers of spacers. Thus, a first gate finger 24A may have a single spacer 40A at approximately the center of the finger 24A and an adjacent finger 24B may have two spacers 40B1, 40B2 centered at about 1/3 and 2/3 the length of the finger 24B. Such a checkerboard pattern 80 may be beneficial in providing a more uniform thermal profile as active portions of adjacent fingers 24A, 24B will be spaced apart from each other in two dimensions. The checkerboard pattern 80 may also reduce the mutual coupling between air bridges.

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently amended) A high power, high frequency semiconductor device comprising:

a plurality of unit cells connected in parallel, the unit cells each having a controlling electrode and first and second controlled electrodes; ~~and~~

a first thermal spacer dividing at least one of the unit cells into a first active portion and a second active portion, spaced apart from the first ~~potion~~ portion by the first thermal spacer, the controlling electrode and the first and second controlled electrodes of the at least one unit cell extending across the first thermal spacer;

a second thermal spacer that divides the at least one unit cell into a third active portion, the third active portion being spaced apart from the first and second active portions and the controlling electrode and the first and second controlled electrodes of the at least one unit cell extending across the second thermal spacer; and

a third thermal spacer dividing an adjacent unit cell into a first active portion and a second active portion, the controlling electrode and the first and second controlled electrodes of the adjacent unit cell extend across the third thermal spacer and wherein the third thermal spacer is offset from the first and second thermal spacers along a direction parallel to the controlling electrode.

2-3. (Cancelled)

4. (Withdrawn) The high power, high frequency semiconductor device of Claim 1, wherein the first and second active portions of the at least one unit cell comprise mesas and wherein the thermal spacer comprises a region between the mesas.

5. (Withdrawn) The high power, high frequency semiconductor device of Claim 4, wherein at least one of the first and/or second controlled electrodes of the at least one unit cell includes an air bridge across the region between the mesas.

6. (Withdrawn) The high power, high frequency semiconductor device of Claim 4, wherein the controlling electrode of the at least one unit cell is provided on sidewalls of the mesas and extends onto a floor of the region between the mesas.

7. (Withdrawn) The high power, high frequency semiconductor device of Claim 4, wherein the mesas comprise epitaxial layers on a substrate and wherein the region between the mesas comprises an exposed region of the substrate.

8. (Original) The high power, high frequency semiconductor device of Claim 1, wherein the thermal spacer comprises an electrically inactive implanted region and/or an insulator region between the first and second active portions of the at least one unit cell.

9. (Currently Amended) ~~The high power, high frequency semiconductor device of Claim 1~~ A high power, high frequency semiconductor device comprising:

a plurality of unit cells connected in parallel, the unit cells each having a controlling electrode and first and second controlled electrodes; and

a thermal spacer dividing at least one of the unit cells into a first active portion and a second active portion, spaced apart from the first portion by the thermal spacer, the controlling electrode and the first and second controlled electrodes of the at least one unit cell extending across the thermal spacer, wherein a cross-sectional area of the controlling electrode is greater where the controlling electrode crosses the thermal spacer than a cross-sectional area of the controlling electrode on the first and second active portions of the at least one unit cell.

10. (Currently Amended) ~~The high power, high frequency semiconductor device of Claim 1~~ A high power, high frequency semiconductor device comprising:

a plurality of unit cells connected in parallel, the unit cells each having a controlling electrode and first and second controlled electrodes; and

a thermal spacer dividing at least one of the unit cells into a first active portion and a second active portion, spaced apart from the first portion by the thermal spacer,

the controlling electrode and the first and second controlled electrodes of the at least one unit cell extending across the thermal spacer, wherein a width of the controlling electrode is greater where the controlling electrode crosses the thermal spacer than a width of the controlling electrode on the first and second active portions of the at least one unit cell.

11. (Original) The high power, high frequency semiconductor device of Claim 1, wherein the thermal spacer is configured to provide a lower peak junction temperature than a corresponding unitary gate device for a particular set of operating conditions.

12. (Original) The high power, high frequency semiconductor device of Claim 1, wherein the unit cells comprise a plurality of unit cells arranged in a linear array.

13. (Original) The high power, high frequency semiconductor device of Claim 1, wherein the controlling electrode comprises a gate finger and the first and second controlled electrodes comprise source and drain electrodes.

14. (Original) The high power, high frequency semiconductor device of Claim 13, wherein the unit cells comprise unit cells of a silicon carbide MESFET.

15. (Original) The high power, high frequency semiconductor device of Claim 13, wherein the unit cells comprise unit cells of a GaN transistor.

16. (Original) The high power, high frequency semiconductor device of Claim 1, wherein the thermal spacer comprises an electrically inactive region configured so as to not generate heat when the semiconductor device is in operation.

17. (Currently Amended) A high power, high frequency field effect transistor, comprising:

a plurality of unit cells electrically connected in parallel, each unit cell having a source region and a drain region;

a plurality of gate electrodes of the unit cells, the plurality of gate electrodes being electrically connected in parallel;

a plurality of source electrodes of the unit cells, the plurality of source electrodes being electrically connected in parallel;

a plurality of drain electrodes of the unit cells, the plurality of drain electrodes being electrically connected in parallel; and

a plurality of thermal spacers that divide corresponding ones of the plurality of unit cells into at least a first active portion and a second active portion and wherein the gate electrodes, source electrodes and drain electrodes of the unit cells cross over the corresponding thermal spacers,

wherein the plurality of thermal spacers are arranged in a checkerboard pattern.

18. (Original) The field effect transistor of Claim 17, wherein the plurality of unit cells comprise a linear array of unit cells.

19. (Cancelled)

20. (Original) The field effect transistor of Claim 17, wherein the plurality of thermal spacers are substantially uniform in size.

21. (Original) The field effect transistor of Claim 17, wherein the plurality of thermal spacers are aligned between adjacent unit cells.

22. (Cancelled)

23. (Original) The field effect transistor of Claim 17, wherein the plurality of unit cells comprise a plurality of silicon carbide unit cells.

24. (Original) The field effect transistor of Claim 17, wherein the plurality of unit cells comprise a plurality of gallium nitride based unit cells.

25. (Withdrawn) The field effect transistor of Claim 17, wherein the first and second active portions of the unit cells comprise mesas and wherein the thermal spacers comprise regions between the mesas.

26. (Withdrawn) The field effect transistor of Claim 25, wherein a least one of the first and/or second controlled electrodes of the unit cells includes an air bridge across the region between the mesas.

27. (Withdrawn) The field effect transistor of Claim 25, wherein the controlling electrodes of the unit cells are provided on sidewalls of the mesas and extend onto floors of the region between the mesas.

28. (Withdrawn) The field effect transistor of Claim 25, wherein the mesas comprise epitaxial layers on a substrate and wherein the regions between the mesas comprise exposed regions of the substrate.

29. (Original) The field effect transistor of Claim 17, wherein the thermal spacers comprise an electrically inactive implanted region and/or an insulator region between the first and second active portions of the unit cells.

30. (Currently Amended) ~~The field effect transistor of Claim 17~~ A high power, high frequency field effect transistor, comprising:

a plurality of unit cells electrically connected in parallel, each unit cell having a source region and a drain region;

a plurality of gate electrodes of the unit cells, the plurality of gate electrodes being electrically connected in parallel;

a plurality of source electrodes of the unit cells, the plurality of source electrodes being electrically connected in parallel;

a plurality of drain electrodes of the unit cells, the plurality of drain electrodes being electrically connected in parallel; and

a plurality of thermal spacers that divide corresponding ones of the plurality of unit cells into at least a first active portion and a second active portion and wherein the gate electrodes, source electrodes and drain electrodes of the unit cells cross over the corresponding thermal spacers,

wherein a cross-sectional area of the ~~controlling~~ gate electrodes is greater where the ~~controlling~~ gate electrodes cross the thermal spacers than a cross-sectional area of the ~~controlling~~ gate electrodes on the first and second active portions of the unit cells.

31. (Currently Amended) ~~The field effect transistor of Claim 17~~A high power, high frequency field effect transistor, comprising:

a plurality of unit cells electrically connected in parallel, each unit cell having a source region and a drain region;

a plurality of gate electrodes of the unit cells, the plurality of gate electrodes being electrically connected in parallel;

a plurality of source electrodes of the unit cells, the plurality of source electrodes being electrically connected in parallel;

a plurality of drain electrodes of the unit cells, the plurality of drain electrodes being electrically connected in parallel; and

a plurality of thermal spacers that divide corresponding ones of the plurality of unit cells into at least a first active portion and a second active portion and wherein the gate electrodes, source electrodes and drain electrodes of the unit cells cross over the corresponding thermal spacers,

wherein a width of the ~~controlling~~ gate electrodes is greater where the ~~controlling~~ gate electrodes cross the thermal spacers than a width of the ~~controlling~~ gate electrodes on the first and second active portions of the unit cells.

32. (Original) The field effect transistor of Claim 17, wherein the thermal spacers are configured to provide a lower peak junction temperature than a corresponding unitary gate device for a particular set of operating conditions.

33. (Original) The field effect transistor of Claim 17, wherein the thermal spacers comprise an electrically inactive region so as to not generate heat when the field effect transistor is in operation.